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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,939	FROUIN ET AL.	
	Examiner	Art Unit	
	Christopher P. Grey	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 4,5,6,7,8,10,11,13,14,18,19,20,21,22,24,25,28,29,30,31,33,36 and 37 are objected to under 37 CFR 1.75(c) as being in improper form as being multiple dependent. See MPEP § 608.01(n). Accordingly, the claim have not been further treated on the merits.

2. Claims 1 and 15 are objected to because of the following informalities: Both claims use the word implements within the preamble, whereas the correct form should be comprising;.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13, 14-28 and 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara et al. (US 6141346), hereinafter referred to as Caldara, in view of Read (US 4542507).

Claim 1, 15, 36, 37, 38 Caldara discloses a synchronization mechanism defining time slots known as connection cycles on at least one of said internal buses (Col 4 lines 7-47);

Caldara discloses a mechanism for writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of elementary data to said selected receiver ports (Col 4 lines 6-22).

Caldara is vague with respect to the description of a mechanism for the allocation of at least one of said connection cycles to each of the selected receiver ports.

Read distinctly discloses a mechanism for the allocation of at least one of said connection cycles to each of the selected receiver ports (Col 9 lines 8-45 and Col 11 lines 28-35).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the timing generator as disclosed by Read (Col 9 line 46-Col 10 line 4) within the ports as disclosed by Caldara. The motivation for this combination is for the control of transmission of data over the bus based on time slots.

Claim 2, 16 Caldara discloses flow control with feedback messages (Col 3 lines 10-20.

However Caldara only vaguely discloses a mechanism comprising a verification step determining whether each of said pieces of elementary data has been received by each of the selected receiver ports.

Read discloses a mechanism comprising a verification step determining whether each of said pieces of elementary data has been received by each of the selected receiver ports (Col 12 line 54-Col 13 line14).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the verification logic unit as disclosed by Read, within the output ports as disclosed by Caldara. The motivation for this modification is to detect failures or potential trouble areas early (Col 1 lines 21-36).

Claim 3, 17, 35 Caldara does not specifically disclose a mechanism for writing

elementary data in each of the allocated connection cycles is reiterated so long as the piece of elementary data has not been received by all the receiver ports.

However, Read discloses a verification logic unit for inserting data into a time slot. Read also discloses the output ports sending either an error signal or

received signal to the verification logic unit (Col 10 lines 22-47), where it would have been an obvious designers choice to repeat the insertion of data into the next cycled time slot on receipt of an error signal, until a received signal occurs.

Claim 4, 18 Caldara discloses the allocation mechanism comprises step of association of each of said connection cycles to each of said selected receiver ports (Col 4 lines 7-22).

Claim 5, 19 Caldara discloses a step for the detection of a transmitter port requesting the transfer of at least one protocol data unit toward at least one selected receiver port, where a scheduled list would depict when and where a transfer of data is necessary (Col 3 lines 57-Col 4 lines 6

Caldara discloses a feedback messaging for flow control thus verifying that the selected receiver ports or ports are ready to receive the protocol data unit or units Col 3 lines 10-20); and

Caldara does not specifically disclose a step for the validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected.

However, Read discloses a step for the validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during the validated connection cycle or cycles when the verification is positive (Col 12 line 54-Col 13 line 14).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the verification logic unit as disclosed by Read, within

the output ports as disclosed by Caldara. The motivation for this modification is to detect failures or potential trouble areas early (Col 1 lines 21-36).

Claim 6, 20, 30, 31, 32 Caldara does not specifically disclose implementing at least one first input bus multiplexing the elementary data coming from at least two transmitter ports and/or at least one first output bus multiplexing said elementary data addressed to at least two receiver ports.

Read discloses implementing at least one first input bus multiplexing the elementary data coming from at least two transmitter ports and/or at least one first output bus multiplexing said elementary data addressed to at least two receiver ports (Col 9 lines 45-Col 10 lines 68).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the multiplexer as disclosed by Read along the bus connecting a transmitter and receiver port as disclosed by Caldara. The motivation for this combination is to allow the transfer of data from different transmitter ports, along the same data bus.

Claim 7, 21 Caldara discloses a port to port connection and a mapping of TSPP (transmitter port)-FSPP (receiver port) as disclosed in Col 3 lines 1-Col 4 lines 5), where it would have been obvious to one of the ordinary skill in the art at the time of the invention that if components within each port are mapped, the ports themselves are paired (also see Read Col 9 lines 7-45).

Claim 8, 22 Caldara discloses the inventions support for point to multipoint connection from an input port to an output port (Col 1 lines 53-64), where it would have been obvious to one of the ordinary skill in the art at the time of the

invention that a port to multi-port connection supports one link from a transmitter port to a receiver port.

Claim 9, 23, 34 Caldara does not specifically disclose the link belonging to the group comprising; the IEEE 1355 equivalent links and the external buses.

Read discloses a number of buses connecting a number of ports (see fig 2), where specifying the links as buses or IEEE equivalent links is routine within the art.

Claim 10, 24 Caldara does not specifically disclose a bit rate greater than or equal to 100 Mbits/s.

Read specifies a bit rate at which data is transferred (Col 5 lines 17-45), where it would have been obvious to one of the ordinary skill in the art at the time of the invention made to specify the links being capable of transferring data at 100 Mbits/s or greater, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233*

Claim 11, 12, 25, 26, 27, 33 Caldara discloses a sub step for the acceptance, by each of the selected received ports, of writing of each piece of elementary data to be transmitted (Col 3 lines 10-21), where available buffers is determined,

Caldara does not specifically disclose second sub step for the transmission of said each piece of elementary data to be transmitted, to each of said selected receiver ports.

Read discloses the second sub step for the transmission of said each piece of elementary data to be transmitted, to each of said selected receiver ports (Col 10 lines 5-21 and Col 12 line 54-Col 13 line 14).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the FSPP for determining if enough buffer space is available as disclosed by Caldara, with the verification logic unit as disclosed by Read, which would receive a feedback message acknowledging availability, and begin writing of data. The motivation for this combination is to detect fault and ensure enough memory is available before the transfer of data.

Claim 13, 28 Caldara discloses the step of arbitration for at least one bus connecting a set of at least one input comprising said transmitted port to a set of at least one output port comprising said receiver ports, said arbitration step being carried out by a switching matrix consisting of crosspoints capable of transmitting elementary data between an input port and an output port, and being organized in rows and columns, each column being capable of managing the reception of elementary coming from an input port associated with the column and each row being capable of managing the transmission of elementary data to an output port associated the the row, so that a single crosspoint per row, at a given point in time, can enable the transmission of elementary data (Col 3 lines 21-Col 4 line 6).

4. Claims 14, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara et al. (US 6141346), hereinafter referred to as Caldara, in view of Read (US 4542507) in further view of Saito et al. (US 6683872), hereinafter referred to as Saito.

Claim 14 The combined teachings of Caldara and Read do not specifically disclose a header, wherein there is an analysis of the header and a modification of the header.

Saito discloses a contents analyzer for analyzing the header of data at an ingress portion of a switch (Col 3 lines 35-40).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the contents analyzer within the combined teachings of Caldara and Read, where the contents analyzer would determine any information within the header such as destination address and control information, and furthermore, the combined teachings of Caldara and Read disclose experiencing an error, where an error may be inserted within the header to indicate a fault in transmission.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Diaz (US 5809021) discloses a multi-service switch for a telecommunications network.

(b) Lam (US 6130891) discloses a multiport switch having management information.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571)272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher Grey
Examiner
Art Unit 2667

3/05

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

11/04/05